REMARKS

Claims 1-18 are pending in the present application. Claims 1, 2, 4, 6 and 7 have been amended. Claims 8-18 have been presented herewith.

Priority Under 35 U.S.C. 119

The Examiner is respectfully requested to acknowledge receipt of the English language translation of the foreign language provisional application submitted on December 29, 2003, and to confirm that the Claim for Priority under 35 U.S.C. 119(e) to U.S. Provisional Application 60/413,782 is complete.

Drawings

Applicants note the Examiner's acceptance of the drawings as filed along with the present application on September 26, 2003.

Specification

The abstract of the disclosure has been objected to as allegedly containing a plurality of paragraphs. However, the abstract as filed along with the present application on September 26, 2003, includes a single paragraph. The Examiner is therefore respectfully requested to withdraw this objection to the abstract.

The Examiner is also respectfully requested to acknowledge receipt and acceptance of the new abstract as submitted herewith.

Claim Rejections-35 U.S.C. 102

Claims 1-5 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Hastings reference (U.S. Patent No. 6,429,723). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The switch circuit of claim 1 includes in combination a first MOS transistor "of a first conductivity type which is coupled between the input terminal and the internal circuit, and which has a control gate receiving a control signal, a first electrode coupled to the input terminal, and a second electrode"; and a second MOS transistor "of a second conductivity type that is opposite the first conductivity type, the second MOS transistor being coupled between the input terminal and the internal circuit, and having a control gate receiving a signal having a phase opposite the control signal, a first electrode coupled to the second electrode of the first MOS transistor, and a second electrode coupled to the internal circuit". Applicants respectfully submit that the Hastings reference as relied upon by the Examiner does not disclose these features.

In view of the current Office Action, NMOS transistor MN1 and PMOS transistor MP1 in Fig. 4 of the Hastings reference would presumably be respectively interpreted as the first MOS transistor of a first conductivity type and the second MOS transistor of a second conductivity type of current claim 1. However, clock Φ_2 in Fig. 4 of the Hastings reference is provided as a control signal input to both MOS transistors MN_1 and MP_1. Accordingly, the circuit in Fig. 4 of the Hastings reference as relied upon by the Examiner, does not include first and second MOS transistors having respective

control signals of opposite phase provided thereto as control signals, as would be necessary to meet the features of claim 1. Applicants therefore respectfully submit that the switch circuit of claim 1 distinguishes over the Hastings reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-5, is improper for at least these reasons.

Claims 1, 6 and 7 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Park et al. reference (U.S. Patent No. 6,566,927). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

In view of the current Office Action, first and second switches 1121 and 1122 in Fig. 11 of the Park et al. reference would presumably be interpreted respectively as the first and second MOS transistors of claim 1. However, first and second switches 1121 and 1122 in Fig. 11 of the Park et al. reference are both illustrated as NMOS transistors, and thus have a same conductivity type. Accordingly, the circuit in Fig. 11 of the Park et al. reference as relied upon by the Examiner does not include first and second MOS transistors having respective different conductivity type, as would be necessary to meet the features of claim 1. Applicants therefore respectfully submit that the switch circuit of claim 1 distinguishes over the Park et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1, 6 and 7, is improper for at least these reasons.

Regarding claim 7, Applicants respectfully disagree with the Examiner's

assertion that the features "an analog circuit" and "a digital circuit" are merely intended use. Contrary to the Examiner's assertion, claim 7 clearly features that "the internal circuit **is** an analog circuit" and that "the another internal circuit **is** a digital circuit". These features are not merely intended use, but specifically describe the circuit type of the internal circuit and the another internal circuit.

The Examiner is respectfully requested to confirm on the record that the above noted features of claim 7 are not merely "intended use", and that these features will be given patentable weight. **In the event that the Examiner maintains the position of record that the above noted features of claim 7 are merely "intended use" and are disregarded, the Examiner is respectfully requested to identify pertinent case law and/or relevant sections of the Manual of Patent Examining Procedure in support thereof.**

Claims 8-18

The switch circuit of claim 8 includes in combination a first MOS transistor "of a first conductivity type having a control gate receiving the control signal, a first electrode connected to the input terminal and a second electrode"; and a second MOS transistor "of a second conductivity type that is opposite the first conductivity type, the second MOS transistor having a control gate receiving an inverted signal having a phase opposite the control signal, a first electrode connected to the second electrode of the first MOS transistor and a second electrode connected to the second internal circuit".

The prior art as relied upon by the Examiner does not disclose first and second MOS transistors of respective different conductivity types and which receive control signals of opposite phase. Applicants therefore respectfully submit that claims 8-13 distiguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

The switch circuit of claim 14 includes in combination a second switch circuit including a first MOS transistor and a second MOS transistor. Applicants respectfully submit that the switch circuit of claim 14 distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 8. Applicants therefore further respectfully submit that the switch circuit of claims 14-18 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

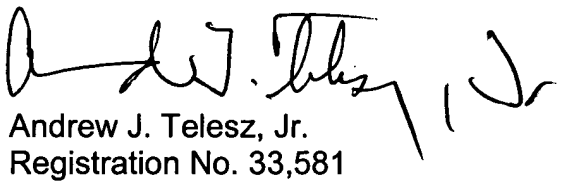
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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